1. A time switch is implemented using the principle given below:

   - Incoming time-slots are written cyclically into a switch memory (SM)
   - Output logic reads cyclically control memory (CM), which contains a pointer for each output time-slot

   Inputs and outputs as well as read/write logic of the memories are expected to be in synchronism.

   What are the required speeds of SM and CM if the switching is dimensioned to support 16 STM-1 input and output links each transporting 63 E1-channels. What are required memory sizes of SM and CM? What about the sizes of input and output buffers? Suppose that SM and CM are shared by all E1s and that there is a memory slot for each time-slot.

2. Consider a 3-stage circuit switched symmetric Clos switching matrix with 1024 input lines. Each input has an average holding time of 280 s and input rate of 1/400 1/s.

   (a) The input is divided into 32 blocks of type 32xk, where k is number of 2nd stage blocks. Use Lee's approximation to find out such k that the blocking probability is < 0.001. What is the total number of switching points?

   (b) What the value of k and the number of the switching points if the switch must be strictly non-blocking?

   (c) What are the optimal (minimal) numbers of 1st and 2nd stage blocks with non-blocking switch. How many switching blocks there are?

3. Consider the crosspoint complexity of three stage Clos networks.

   (a) Show that the strict-sense network has roughly twice the complexity of the rearrangeable network.

   (b) For the rearrangeable network, show that the optimal choice of p (slide 4-44) for minimising crosspoint count is $\sqrt{N/2}$, which gives a crosspoint complexity of $2\sqrt{2}N^{3/2}$.

   (c) For the strict sense network (slide 4-45), show that the minimum crosspoint count is roughly given by $4\sqrt{2}N^{3/2}$.

4. Consider a symmetric 6×6 SSS-switch where 1st and 3rd stages are composed of 2×2 switching blocks.

   (a) Determine the size and number of 2nd SBs.

   (b) Draw a graph presentation for the switch.

   (c) Allocate paths for connections $t_1 \to r_3$, $t_2 \to r_6$, $t_4 \to r_1$, and $t_6 \to r_5$.